

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

**Title of
Invention**

Embedded Processor with Watchdog Timer for Programmable
Logic

Application Number : 10-711137

Confirmation Number:

First Named Applicant: Andrew Crosland

Attorney Docket Number: 15114-053510

Art Unit:

Examiner:

Search string: (5687325 or 6260087 or 6467009 or RE34444 or 5970254),pn

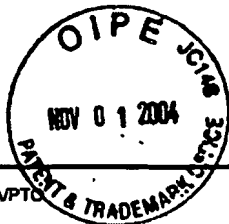
US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
H7D	1	5687325	1997-11-11	Web Chang			
	2	6260087	2001-07-10	Web Chang			
	3	6467009	2002-10-15	Winegarden			
	4	RE34444	1993-11-16	Kaplinsky			
	5	5970254	1999-10-19	Cooke			

Signature

Examiner Name Date



PTO/SB/08A (08-03)

Substitute for form 1449A/PTO		INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known	
				Application Number	10/711,137
		Filing Date	August 27, 2004		
		First Named Inventor	Crosland, Andrew		
		Art Unit	Unassigned	2875	
		Examiner Name	Unassigned	DIM 7/8/04	
Sheet	1	of	3	Attorney Docket Number	015114-053510US

U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
M7D	AA	US-4,488,259	12-11-1984	Mercy	
	AB	US-4,617,479	10-14-1986	Hartmann et al.	
	AC	US-4,710,927	12-01-1987	Miller	
	AD	US-4,871,930	10-03-1989	Wong et al.	
	AE	US-5,241,224	08-31-1993	Pedersen et al.	
	AF	US-5,258,668	11-02-1993	Cliff et al.	
	AG	US-5,260,610	11-09-1993	Pedersen et al.	
	AH	US-5,260,611	11-09-1993	Cliff et al.	
	AI	US-5,412,260	05-02-1995	Tsui et al.	
	AJ	US-5,436,575	07-25-1995	Pedersen et al.	
	AK	US-5,550,782	08-27-1998	Cliff et al.	
	AL	US-5,790,479	08-04-1998	Conn	
	AM	US-6,097,211	08-01-2000	Couts-Martin et al.	
	AN	US-6,233,205	05-15-2001	Wells et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
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Examiner Signature		Date Considered	5/30/07
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/711,137
				Filing Date	August 27, 2004
				First Named Inventor	Crosland, Andrew
				Art Unit	Unassigned <i>2825</i>
				Examiner Name	Unassigned <i>DIH70N</i>
Sheet	2	of	3	Attorney Docket Number	015114-053510US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>M-fn</i>	AO	AITKEN, R.C., and AGARWAL, V.K., "A Diagnosis Method Using Pseudo-Random Vectors Without Intermediate Signatures," Proc. of Int. Conf. on Computer-Aided Design (ICCAD), IEEE pp. 574-577 (1989).	
	AP	Altera "APEX 20K Programmable Logic Device Family Data Sheet," May 1999, 7 pages total.	
	AQ	Altera "FLEX 10K Embedded Programmable Logic Family Data Sheet," May 1999, 7 pages total.	
	AR	Altera "FLEX 8000 Programmable Logic Device Family Data Sheet," May 1999, 5 pages total.	
	AS	Altera "IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices," August 1999, Application Note 39, 29 pages total.	
	AT	Altera "MAX 7000 Programmable Logic Device Family Data Sheet," May 1999, 6 pages total.	
	AU	"AT94K Series Field Programmable System Level Integrated Circuit," Advance Information Brochure of Atmel Corporation, December 1999, 6 pages.	
	AV	"CS2000 Reconfigurable Communications Processor Family Product Brief," Advance Product Information from ChameleonSystems, Inc., 2000, pages 1-8	
	AW	DeHON, DPGA-Coupled Microprocessors: Commodity ICs for the Early 21st Century, Artificial Intelligence Laboratory, Massachusetts Institute of Technology, Cambridge, MA, IEEE, February, 1994, pp. 31-33	
	AX	GHOSH-DASTIDAR, J., and TOUBA, N.A., "A Rapid and Scalable Diagnosis Scheme for BIST Environments With a Large Number of Scan Chains," Proc. of IEEE VLSI Test Symposium, pp. 79-85 (2000).	
	AY	GHOSH-DASTIDAR, J., DAS, D., and TOUBA, N.A., "Fault Diagnosis in Scan-Based BIST using Both Time and Space Information," Proc. of International Test. Conf., IEEE, pp. 95-102 (1999).	
	AZ	HAUSER, and WAWRZYNEK, University of California, Berkeley, "Garp: A MIPS Processor with a Reconfigurable Coprocessor," IEEE, April 1997, pp. 12-21.	
	BA	IBM Corporation, "Mixture of Field and Factory Programmed Logic Cells in a Single Device," IBM Technical Disclosure Bulletin, April 1995, pp. 499-500	
	BB	MC ANNEY, M.G. and SAVIR, J., "There is Information in Faulty Signatures," Proc. of International Test Conf., IEEE, pp. 630-636 (1987).	
	BC	"Motorola Technical Developments," Magazine of Motorola, Inc., Vol. 39, September 1999, pp. i-vii and 77-80.	
	BD	NAGEL, "ACM Computing Surveys: Synergy Between Software and Hardware," Carnegie Mellon University, Department of Electrical Engineering and Computer Science, Pittsburgh, PA, December, 1996, pp. 1-3.	

Examiner Signature	<i>[Signature]</i>	Date Considered	<i>5/26/07</i>
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449B/PTO		Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/711,137
		Filing Date	August 27, 2004
		First Named Inventor	Crosland, Andrew
		Art Unit	Unassigned 2828
		Examiner Name	Unassigned DPH/TAK
Sheet	3	of	3
		Attorney Docket Number	015114-053510US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
M-T	BE	RAZDAN, and SMITH, "A High-Performance Microarchitecture with Hardware-Programmable Functional Units," Harvard University, Cambridge, MA, Digital Equipment Corporation, Hudson, MA, November, 1994, pp. 172-180.	
	BF	"Triscend E5 Configurable System-on-Chip Family," Product Description from Triscend Corporation, January, 2000 (Version 1.00), pp. I-II and 1-90.	
	BG	"Wireless Base Station Design Using Reconfigurable Communications Processors," Wireless Base Station White paper from ChameleonSystems, Inc., 2000, pages 1-8.	
	BH	WITTIG, and CHOW, "OneChip" An FPGA Processor With Reconfigurable Logic," Department of Electrical and Computer Engineering, University of Toronto, Ontario, Canada, IEEE, September, 1996, pp. 126-135.	
	BI	WYNN, "In-Circuit Emulation for ASIC-Based Designs," Xilinx, Inc., VLSI Systems Design, October, 1986, pp. 38-39, and 42-45.	

Examiner Signature		Date Considered	5/20/07
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